REMARKS

Claims 1-22 were pending in the present application. Claims 4, 5, 15, and 16 have been cancelled. Claims 1-3, 6, 9-14, 17, 21, and 22 have been amended. Accordingly, claims 1-3, 6-14, and 17-22 are now pending in the application.

The drawings are objected to for including reference numbers not referenced in the specification. The drawings have been amended as described above.

The specification is objected to for using an acronym without first defining the acronym. Applicant has corrected the specification as requested.

Claims 1-11 stand rejected under 35 U.S.C §112, 2nd paragraph, as being indefinite. Applicant has amended the claims and believes the rejection to now be moot.

Claim 22 stands rejected under 35 U.S.C. §101 for being directed to non-statutory subject matter. Applicant respectfully traverses this rejection.

Applicant respectfully submits that a rejection under 35 U.S.C. §101 is improper since claim 22 is directed to a processor, which clearly falls within the scope of an apparatus claim which is one of the statutory categories. In addition, as to whether the claim is of proper form, Applicant directs the Examiner to 35 U.S.C. §112, 6th paragraph, which states "An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification." Accordingly, Applicant submits claim 22 is directed to statutory subject matter, and the claim is of the proper form. Thus, Applicant respectfully requests the rejection of claim 22 under 35 U.S.C. §101 be withdrawn.

Claims 1-16, and 21-22 stand rejected under 35 U.S.C. §102(b) as being anticipated by Emer et al. (U.S. Patent No. 6,073,159) (hereinafter "Emer"). Although Applicant respectfully traverses at least portions of this rejection, Applicant has amended the claims to expedite allowance.

Claims 17-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Emer in view of Keats et al. (U.S. Patent No. 6,167,461) (hereinafter "Keats"). Although Applicant respectfully traverses at least portions of this rejection, Applicant has amended the claims to expedite allowance.

Applicant's claim 1 recites a processor comprising in pertinent part,

> "a detection unit coupled to the execution unit and configured to detect whether a given thread includes a specific identifier;
>
> wherein said execution unit is further configured to selectively continue execution of said given thread depending upon whether said detection unit detects said specific identifier;
>
> wherein said execution unit is configured to suspend execution of said given thread and to execute a different thread in response to receiving a global execution parameter; and
>
> wherein in response to said detection unit detecting said specific identifier, said execution unit is configured to override said global execution parameter and to continue execution of said given thread."
> (Emphasis added)

Emer discloses at col. 5, lines 36-46

> "Each instruction is assigned a unique number, called an instruction identifier, which is used to identify the instruction and its program order with respect to other instructions during the time the instruction is in flight. An instruction is considered to be in flight when it enters the fetch stage 42 and is no longer in flight once it is cancelled due to, for instance, a branch mispredict or once it has completed the commit stage 54 which will be discussed below. In addition, a thread identifier, which is used to

identify the thread with which the instruction is associated, is also assigned to each instruction during the fetch stage 42." (Emphasis added)

Emer also discloses at col. 6, lines 31-44

> "These attributes represent, for example, a probability of an instruction from a thread subsequently being cancelled after it has entered the pipeline or a probability of a thread filling the instruction queue with unissuable instructions, thus restricting fetch and issue throughput. This restriction of fetch and issue throughput is typically referred to as instruction queue clog. These collected attributes are examined to make an educated selection of a subsequent thread from which to fetch instructions. **A thread is selected if it is not suffering from an adverse attribute**. That is, a thread would not be preferred for selection if it has a high probability of experiencing a branch mispredict, which would result in an instruction or instructions subsequently being cancelled, or if it has a high probability of causing an instruction queue clog." (Emphasis added)

Emer further discloses at col. 8, lines 44-56

> "Referring now to FIG. 5A, a thread A bit vector 70, used to implement the BRCOUNT, MISSCOUNT, ECOUNT and ICOUNT schemes, is shown to include an entry for each instruction from thread A resident in one of the pipeline stages of computer system 10. A similar bit vector is provided for each of the remaining threads B-H executing within computer system 10 and is used to collect information representing attributes for the thread in accordance with the currently implemented fetching scheme. Here, bit vector 70 is implemented as special purpose hardware, typically including a bank of set-reset flip flops.
> The bit vector 70 is indexed by the instruction identifier, for each instruction." (Emphasis added)

Emer further discloses at col. 10, lines 18-37

> "Referring now to FIG. 5B, a bit vector 92a-92h for each of the threads executing within computer system 10 is shown. The entries in each of the bit vectors 92a-92h correspond to each location within the instruction queue 30 (FIG. 2) where an instruction is resident. That is, each bit vector includes a bit corresponding to each location in the instruction queue 30 currently occupied by an instruction. For each instruction in the instruction queue 30, a bit is set in the bit vector corresponding to the thread to which that instruction belongs. In this manner, the set bit indicates both the thread to which the instruction belongs as well as the instruction's location in the instruction queue relative to the head of the instruction queue. As instructions are removed from the instruction queue, the corresponding bit in the bit vector is cleared. In addition, as the location of the instruction in

> the instruction queue 30 changes so will the location of the set bit in the bit vector 92.
> To determine which thread to select under the IQPOSN scheme, the bit vectors 92a-92h are first evaluated to determine the location of the leading instruction. That is, each bit vector 92a-92h is evaluated to determine at which location in the instruction queue 30, does the first instruction belonging to that thread reside." (Emphasis added)

From the foregoing disclosures it is clear that Emer is disclosing a scheme for choosing a given thread for execution from a number of possible threads to execute. However, in contrast to the Examniner's assertion that Emer teaches detecting whether an instruction has an identifier, Applicant submits Emer ascertains whether the attributes that are present constitute adverse attributes to being selected. Emer does not detect whether a given instruction has an identifier. Clearly from above, all instructions have identifiers that index into at least one bit vector that holds attributes for the instruction/and or thread. Moreover, the thread is being evaluated for execution, not whether to continue execution as recited in claim 1.

In addition, in regard to the Examiner's rejection of claims 4 and 5, Applicant respectfully submits the features recited in those claims is not taught or suggested in Emer as suggested by the Examiner. More particularly, Emer teaches at col. 4, lines 27-29

> "Both the completion of instructions and the cancelling of instructions are done on a per thread basis. Accordingly, each instruction is also provided a thread identifier which allows an instruction from one thread to be distinguished from instructions associated with another thread."

and at col. 6, lines 31-38 as shown above.

Applicant submits that from the foregoing disclosure, Emer does not mention a global execution parameter. Since a global execution parameter is one which gives the processor an unconditional directive to execute instructions in a certain way in the absence of an identifier.

Further, Emer discloses at col. 1, lines 9-12

> "One type of CPU is an in-order execution CPU. In an in-order execution CPU, instructions in an instruction stream are executed in the order in which they occur in the instruction stream. In an out-of-order execution CPU, instructions in the instruction stream are identified which are not dependent upon other instructions in the instruction stream."

Applicant resectfully submits this does not teach or disclose overriding a global execution parameter when a specifc identifier is detected. Applicant sees no relevance to overriding a global execution parameter when a specific identifier is detected whatsoever.

Accordingly, Applicant submits claim 1, along with its dependent claims patentably disticguishes over Emer for the reasons given above.

Applicant's claims 12, 21, and 22 recite features that are similar to claim 1. Accordingly, Applicant submits claims 12, 21, and 22, along with their respective dependent claims patentably distinguish over Emer for at least the reasons given above.

Applicant's claim17 recites features that are similar to claim 1. Further, Keats is not relied upon nor does Keats teach the combination of features recited in Applicant's claim 17. Thus, Applicant submits claim 17, along with its dependent claims patentably disticguishes over Emer in view of Keats for the reasons given above.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-72500/SJC.

Respectfully submitted,

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